Interview Questions asked in various Companies

Western Digital:

* Practical techniques to solve Setup violations.
* CDC techniques in detail
* Write a Verilog code for asynchronous FIFO
* How you are writing pipeline code what problems occur and how did you resolve it?
* Which scripting language do you use for tools?
* For AXI, which language was used in your previous company?

Cisco:

* Write a constraints for 4k address space, 5% in lower 1k, 5% in upper 1k.
* Write a virtual task so these signals can be transferred from Driver to DUT via interface

Memory\_seq\_item:

rand bit[7:0] addr;

rand bit wr\_en;

rand bit rd\_en;

rand bit [31:0] wr\_data;

bit [31:0] rd\_data, clk, reset;

Code a virtual task drive () with req, `DRIVE\_IF.(This is a driver class)

* What are the signals of the channel from which I would like to transfer this data “Increment burst type, 3 transfers, 4 bytes per transfer, start at address 0”. Now write the values of signal burst\_type, awsize, and awlen for the above-mentioned question.

Qualcomm:

* Fork join, Fork- join\_any, fork join\_none.
* Explain UVM virtual sequence, virtual sequencer
* What is TLM FIFO.
* Swap x &Y with and without temp variable.
* Have you worked on agent.

Johnson& Johnson

* Difference between ASIC and FPGA design Flow.
* Difference between combinational and sequential circuits.
* What is timing analysis and what is the requirement for FPGA.
* What is soft constraints.
* How to make a soft constraint
* Write a forecah loop in the constraint
* Generate a unique array without using a unique keyword in randomization.
* Define all protocols.
* Difference between new() and create.
* Arrays and queue-related questions
* Virtual sequence and virtual sequencer
* Constraint to generate unique values in array out of order.

Qualcomm:

* AXI protocol channels
* Turn on and off power in python
* Append and extend difference in python
* Match case and switch case difference.
* Difference between moore and mealy
* Master of AXI has given and asked to design a slave
* Design FSM through VALID AND READY SIGNAL

Synopsys and Intel:

* Difference between System Verilog and Verilog.
* Why do you feel like moving to SV?
* Difference between bit and logic data type.
* Reg, wire and logic difference.
* Thought process on MIPS32 processor
* How to read and write happen in cache.
* PCI protocol
* Explain the Zebu simulator
* What have you done in the simulation
* Team project or individual, whats your preference?
* How do you interact with cross-functional team?
* 5 stages of the pipeline
* Have you done SV validation
* Types of coverage
* Types of code coverage
* UVM components and objects difference
* 0101 pattern detection with and without FSM and write the Verilog code
* Sequential and combinational circuit
* Why sensitivity list is important in Verilog
* Circuit difference when using IF/ELSE and CASE statement.
* Latch and FF difference
* Synchronous and asynchronous circuits difference.
* Metastability ? and how we can avoid it.
* Casex and case z
* Task and function
* Parameter and defparam
* Mailbox and queue difference
* Polymorphism
* When to use dynamic array and associative array.
* System tasks in Verilog
* Sequence detector
* What does this code is doing?
  + always@(posedge a or posedge b) begin
    - if (a)
      * y<= 1’b0;

else if (c)

y<=d;

else

y<=y

* D flipflop code with synchronous reset and asynchronous reset
* Blocking and nonblocking difference
* == and === difference
* Clock gating techniques
* Full case and parallel case
* Data synchronizer
* What is setup and hold violation, propagation delay.
* What is 4-bit values
* Why latch is not good for design.
* Inferred latch vs combinational loops
* Difference between Moore and mealy.
* Modifiers priority and unique keyword.
* Always\_latch and always\_comb
* What is the Frequency of pipeline and nonpipelined processor
* Hazards in the pipeline
* Frequency divider (F/2, F/8, F/5 and F/7).
* RTL code of DFF AND Counter.
* Asynchronous and synchronous reset
* How Z works on FPGA
* sta constraints in tool
* Why hold is not time dependent
* Is it okay to increase frequency divider or how to doo it.
* Purpose of Reset synchronizer
* Dual Edge Flipflop
* Inverte and buffer from XOR
* MOD8 to MOD6 conversion
* D latch to JK Latch
* 1 bit counter or toggle counter
* How many 2:1 MUX is required for 128:1 MUX
* FPGA and ASIC Design Flow
* how do you choose fpga.
* what should keep in mind while working with fpga
* distributed and block RAM memory
* Slice L and Slice M in FPGA
* Single port and dual port ram
* Static timing analysis
* Maximum clock frequency of Counter
* Which violation is more dangerous
* Full adder without HA
* How to implement adder in MIPS32
* FIFO Depth
* Make logic gates using MUX
* 3 bit asynchronous counter
* Limitation of asynchronous counter
* Positive and negative edge detector
* Race around condition example
* Pulse stretcher and pulse compressor
* Grey to binary and viceversa
* Why grey consume lesss power
* Application of grey code
* When to use data synchronizer,
* Types of counter and then difference between ring and johnson counter
* Up and down counter
* What is interface, assertions, classes , code coverage in sv/
* Difference between procedural and concurrent blocks in sv
* Difference between static function and function static
* Create queue then find size, push pop.
* Write string in SV